WHAT IS CLAIMED IS:

1. A memory testing system comprising:

a first memory tester which detects failed location information from a memory at a first frequency;

an interface in communication with the first memory tester; and

a second memory tester, in communication with the interface, which receives the failed location information at a second frequency.

2. The memory testing system according to claim 1, wherein the first frequency is the memory operating frequency.

3. The memory testing system according to claim 1, wherein the second frequency is the working frequency of the second memory tester.

4. The memory testing system according to claim 1, wherein the first memory tester comprises a built-in self-test (BIST).

5. The memory testing system according to claim 1, wherein the first memory tester comprises a CPU.

6. The memory testing system according to claim 1, wherein the second memory tester comprises an external memory tester.

7. The memory testing system according to claim 1, wherein the first frequency is higher than the second frequency.

8. The memory testing system according to claim 1, wherein the interface comprises a general processor input/output (GPIO) interface.

9. The memory testing system according to claim 1, wherein the first memory tester asserts busy after receiving a test start signal.

10. The memory testing system according to claim 1, wherein the second memory tester sends N clocks of data strobes at the second frequency to the interface upon detection of a failed memory location.

11. The memory testing system according to claim 10, wherein the value of N is the minimum number of data strobe cycles required to clock out all necessary information for a failed memory location.

12. The memory testing system according to claim 11, wherein the first memory tester asserts error when a failed memory location is detected, and de-asserts error before N-1 clocks of data strobes.

13. A method for testing a memory in a system comprising a first memory tester, a second memory tester, and an interface in communication with the first and second memory tester, the method comprising:

transferring failed location information from the memory to the first memory tester at a first frequency; and

transferring the failed location information over the interface to the second memory tester at a second frequency that is lower than the first frequency.

14. The method according to claim 13, wherein the first frequency is the memory operating frequency.

15. The method according to claim 13, wherein the second frequency is the working frequency of the second memory tester.

16. A memory testing system comprising:

means for detecting failed location information from a memory at a first frequency;

means for receiving the failed location information at a second frequency; and

means for enabling the detecting means and the receiving means to communicate with each other.

17. The memory testing system according to claim 16, wherein the first frequency is the memory operating frequency.

18. The memory testing system according to claim 16, wherein the second frequency is the working frequency of the receiving means.

19. The memory testing system according to claim 16, wherein the detecting means comprises a built-in self-test (BIST).

20. The memory testing system according to claim 16, wherein the detecting means comprises a CPU.

21. The memory testing system according to claim 16, wherein the receiving means comprises an external memory tester.

22. The memory testing system according to claim 16, wherein the first frequency comprises higher than the second frequency.

23. The memory testing system according to claim 16, wherein the communication enabling means is a general processor input/output (GPIO) interface.

24. The memory testing system according to claim 16, wherein the detecting means asserts busy after receiving a test start signal.

25. The memory testing system according to claim 16, wherein the receiving means sends N clocks of data strobes at the second frequency to the communication enabling means upon detection of a failed memory location.

26. The memory testing system according to claim 25, wherein the value of N is the minimum number of data strobe cycles required to clock out all necessary information for a failed memory location.

27. The memory testing system according to claim 26, wherein the detecting means asserts error when a failed memory location is detected, and de-asserts error before N-1 clocks of data strobes.

28. A method for reducing data reporting during memory testing, the method comprising:

storing an address of a first failed memory location in a first failed memory location storage device when the first failed memory location is unique;

comparing an address of a second failed memory location with the address stored in the first failed memory location storage device; and

continuing memory testing without reporting the second failed memory location when the address of the second failed memory location matches the address stored in the first failed memory location storage device, if the address stored in the first failed memory location storage device has been matched for more than a predetermined number of times.

29. The method according to claim 28, further comprising:

when the address of the second failed memory location matches the address stored in the first failed memory location storage device, storing the second failed memory location in a second failed memory location storage device.

30. The method according to claim 29, further comprising:

when the second failed memory location is stored in the second failed memory location storage device, indicating that the address stored in the first failed memory location storage device is matched one more time.

31. The method according to claim 28, wherein the capacity of the first failed memory location storage device depends on available redundant resources.

32. The method according to claim 28, further comprising:

flagging the memory as irreparable when the first failed memory location storage device is full.

33. The method according to claim 28, wherein the predetermined number is X+1, and wherein X is the number of available redundant column.

34. The method according to claim 28, wherein the predetermined number is Y+1, and wherein Y is the number of available redundant row.

35. The method according to claim 29, wherein the first failed memory location storage device and the second failed memory location storage device are the same.

36. An apparatus for performing the method according to claim 28, comprising:

the first failed memory location storage device for storing the address of the first failed memory location when the first failed memory location is unique;

a comparator for comparing the address of the second failed memory location with the address stored in the first failed memory location storage device; and

a decision unit for deciding whether to report the second failed memory location.

37. The apparatus according to claim 36, further comprising:

the second failed memory location storage device for storing the second failed memory location.

38. The apparatus according to claim 36, further comprising:

an indicator for indicating that the address in the first failed memory location storage device has been matched one more time.

39. The apparatus according to claim 36, wherein the capacity of the first failed memory location storage device depends on available redundant resources.

40. The apparatus according to claim 36, further comprising:

an indicator for indicating that memory is irreparable when the first failed memory location storage device is full.

41. The apparatus according to claim 36, wherein the predetermined number is X+1, and wherein X is the number of available redundant column.

42. The method according to claim 36, wherein the predetermined number is Y+1, and wherein Y is the number of available redundant row.

43. The apparatus according to claim 37, wherein the first failed memory location storage device and the second failed memory location storage device are the same.

44. An apparatus for performing the method according to claim 28, comprising:

a first storing means for storing the address of the first failed memory location when the first failed memory location is unique;

means for comparing the address of the second failed memory location with the address stored in the means for storing the address of the first failed memory location; and

means for deciding whether to report the second failed memory location.

45. The apparatus according to claim 44, further comprising:

a second storing means for storing the address of the second failed memory location.

46. The apparatus according to claim 44, further comprising:

meaning for indicating that the address in the first storing means has been matched one more time.

47. The apparatus according to claim 44, wherein the capacity of the first storing means depends on available redundant resources.

48. The apparatus according to claim 44, further comprising:

means for indicating that memory is irreparable when the first storing means is full.

49. The apparatus according to claim 44, wherein the predetermined number is X+1, and wherein X is the number of available redundant column.

50. The method according to claim 44, wherein the predetermined number is Y+1, and wherein Y is the number of available redundant row.

51. The apparatus according to claim 45, wherein the first storing means and the second storing means are the same.

52. A memory testing system, comprising:

a memory tester for detecting failed memory location information from the memory; and

the apparatus according to claim 36.

53. A memory testing system, comprising:

a memory tester for detecting failed memory location information from the memory; and

the apparatus according to claim 44.

54. A method for allocating redundant resources to repair failed memory locations, wherein the redundant resources includes X columns and Y rows, the method comprising:

when a first failed memory location is unique, storing an address of the first failed memory location in a first failed memory location storage device;

when an address of a second failed memory location matches the address stored in the first failed memory location storage device, storing the second failed memory location in a second failed memory location storage device; and

classifying the failed memory locations.

55. The method according to claim 54, further comprising:

indicating that there are more than X failed memory locations in the same row of the memory.

56. The method according to claim 55, further comprising:

classifying the row that has X failed memory locations as errors with highest priority.

57. The method according to claim 56, further comprising:

allocating a redundant row to replace the row that has X failed memory locations.

58. The method according to claim 54, further comprising:

indicating that there are more than Y failed memory locations in the same column of the memory.

59. The method according to claim 58, further comprising:

classifying the column that has Y failed memory locations as errors with highest priority.

60. The method according to claim 59, further comprising:

allocating a redundant column to replace the column that has Y failed memory locations.

61. The method according to claim 54, further comprising:

indicating that there is more than one failed memory location in the same row of the memory.

62. The method according to claim 54, further comprising:

indicating that there is more than one failed memory location in the same column of the memory.

63. The method according to claim 54, further comprising:

when there are four failed memory locations forming a rectangle, classifying the four failed memory locations as errors with the second highest priority.

64. The method according to claim 63, further comprising:

repairing the four failed memory locations without using a column.

65. The method according to claim 63, further comprising:

repairing the four failed memory locations without using a row.

66. The method according to claim 54, further comprising:

when a failed memory location is a single bit error, classifying the failed memory location as an error with the lowest priority.

67. The method according to claim 66, further comprising:

repairing the failed memory location by either a row or a column, according to the remaining available redundant resource.

68. The method according to claim 54, wherein the first failed memory location storage device and the second failed memory location storage device are the same.

69. An apparatus for performing the method according to claim 54, comprising:

the first failed memory location storage device for storing the address of the first failed memory location when the first failed memory location is unique;

the second failed memory location storage device for storing the second failed memory location when the address of the second failed memory location matches the address in the first failed memory location storage device; and

a classifier for classifying the failed memory locations.

70. The apparatus according to claim 69, further comprising:

an indicator for indicating that there are more than X failed memory locations in the same row of the memory.

71. The apparatus according to claim 69, further comprising:

an indicator for indicating that there are more than Y failed memory locations in the same column of the memory.

72. The apparatus according to claim 69, further comprising:

an indicator for indicating that there is more than one failed memory location in the same row of the memory.

73. The apparatus according to claim 69, further comprising:

an indicator for indicating that there is more than one failed memory location in the same column of the memory.

74. The apparatus according to claim 69, wherein the first failed memory location storage device and the second failed memory location storage device are the same.

75. An apparatus for performing the method according to claim 54, comprising:

a first storing means for storing the address of the first failed memory location when the first failed memory location is unique;

a second storing means for storing the second failed memory location when the address of the second failed memory location matches the address in the first storing means; and

means for classifying the failed memory locations.

76. The apparatus according to claim 75, further comprising:

means for indicating that there are more than X failed memory locations in the same row of the memory.

77. The apparatus according to claim 75, further comprising:

means for indicating that there are more than Y failed memory locations in the same column of the memory.

78. The apparatus according to claim 75, further comprising:

means for indicating that there is more than one failed memory location in the same row of the memory.

79. The apparatus according to claim 75, further comprising:

means for indicating that there is more than one failed memory location in the same column of the memory.

80. The apparatus according to claim 75, wherein the first storing means and the second storing means are the same.

81. A memory testing system, comprising:

a memory tester which detects failed memory location information from the memory; and

an apparatus for allocating redundant resources according to claim 69.

82. A memory testing system, comprising:

a memory tester which detects failed memory location information from the memory; and

an apparatus for allocating redundant resources according to claim 75.